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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/821,564	LANDIN ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14,17-20,22-27 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-14,17-20,22-27 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 7/6/2007. Claims 2,15,16,21, and 28-33 are cancelled, and claims 1,3-14,17-20,22-27 and 34 remain pending. Applicant's arguments and amendments have been carefully considered, but they are not persuasive and do not place the claims in condition for allowance. Accordingly, this action has been made FINAL.

Claim Objections

Claim 3 is objected to because of the following informalities:

A period needs to be placed at the end of claim 3.

Claim 3 is further objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. With the present amendment of portions of claim 4 into claim 1, claim 3 does not further limit claim 1.

Appropriate correction is required.

Response to Amendment/Arguments

Applicant's amendments to the independent claims have changed the scope of the claims. Upon a cursory search of the prior art, the reference of Van Doren was uncovered and applied in the rejection that follows to teach the claimed limitation of delaying the data of a cache line at the interface until all invalidation acknowledgements from processors sharing that cache line are received before forwarding the data on the data bus for the requesting processor.

Further, the prior art reference of Singhal has been cited to teach the claimed limitation of the address packet and the data packet both being part of a transaction initiated by a processor requesting a cache line.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3-14,17-20, 22-27, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo et al (U.S. Patent Application Publication No. 2002/0124144) in view of (Singhal et al. (U.S. Patent No. 5,987,874) in further view of Van Doren et al. (U.S. Patent No. 6,209,065).

As per claims 1,19, and 34, Gharachorloo teaches:

(1) a node 102 in figure 1 which includes a processing subsystem (combination of CPU 106 and associated caches 108 and 110) and an interface (combination of elements

122,124,136,130,12, and 128) coupled by an address network and a data network (112 as well as interconnects that couple the components of the interface together), since the interface is capable of sending and receiving both data and address requests/responses (¶158);

(2) an additional node 102, 104 including an additional processing subsystem (106,108,110) and an additional interface (as define above) coupled by an additional address network and an additional data network (as defined above) - ¶49 teaches multiple nodes are components of the system of figure 1;

(3) an inter-node network 134 configured to convey communications between the node and the additional node, wherein the interface and the additional interface are coupled to send and receive communications on the inter-node network - ¶50;

(4) Gharachorloo does not specifically teach as part of the coherency transaction involving a coherency unit cached by the processing subsystem, the processing subsystem being configured to transaction an access right to the coherency unit *in response to the processing subsystem receiving a data packet via the data network* and to transition an ownership responsibility for the coherency unit *in response to an address packet on the address network* wherein the processing subsystem transitions the access right at a different time than the ownership responsibility.

Singhal teaches such cache coherence with respect to [27/50 - 28/30]. A processing subsystem (e.g. board) may become the owner of the cache line as soon as it requests ownership using a readtoown address packet [27/64-66]; therefore, in response to an address packet on the address network, ownership transition occurs. Singhal further teaches a processing subsystem may be granted an access right (e.g. authorship [28/3-11], the ability to write the cache line)

when the actual data is received by the processor; therefore, in response to a data packet on the data network, an access right transition occurs. Singhal teaches such an approach to disassociate ownership with the reception of the data packet, alleviates cache line owners of other systems from having to respond to requests for ownership within a small window allotted for data transfer [27/55-62]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the cache coherency system of Gharachorloo with the ownership/access right transition timing system of Singhal in order to have alleviated the difficulty of transferring data ownership and access rights for data in the system of Gharachorloo by a single owner is such a small window of data transfer.

Singhal further teaches that the address packet and the data packet are part of a transaction initiated by the processing subsystem - [27/64 - 28/11] - (a ReadToOwn transaction supplies an address on the address bus for ownership and receives the data on the data bus when it is relinquished by the previous owner).

Neither Gharachorloo or Singhal teach specifically teach the interface in the node is configured to delay providing the data packet on the data network until the interface receives an indication that shared copies of the coherency unit in the additional node have been invalidated. Gharachorloo teaches (¶181) that the cache line is forwarded immediately from the RCE 124 (interface) to the requesting processing when it is received along with an indication that the transaction is not complete (as other processors need to invalidate their copy of the requested cache line). Once all of the acknowledgements have been received, the RCE sends an additional message (¶182) to the processor indicating that the transaction is complete and that the cache line may now be written to (e.g. access right obtained). Such a method involves an additional

message being sent to the requesting processor and therefore and increase in the traffic of the data bus between the RCE interface and the processors.

Conversely, Van Doren teaches a controller (180 figure 1, e.g. an interface) regulates a request by a processor to obtain exclusive rights for a cache line [19/6-21]. Only after the FrdMod x probe (e.g. the data from the previous owner of the cache line) and all invalidation acknowledgements have been received, will the controller forward the data to the requesting processor.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the cache coherency system of modified Gharachorloo with the teaching of delaying the transfer of data to a requesting processor until all invalidation acknowledgements have been made by other processors in order to have (1) lowered the messaging traffic between the interface and the processors, thereby increasing the bandwidth of the bus and (2) ensured that the requesting processor would not violate cache coherency by writing to the cache line before other processors had invalidated their copies.

As per claim 3, the interface (specifically, the RPE 124) in the node is configured to delay providing --data corresponding to the coherency unit-- on the data network (switch 112) until the interface has received an indication that shared copies of the coherency unit in the additional node (in this case either the home node or owner node) have been invalidated - as taught by Van Doren [19/6-21] as discussed in the rejection of claim 1 above.

As per claim 4, the data packet received by the processing subsystem is conveyed on the data network by the interface 112 as part of a read-to-own transaction (read-exclusive

transaction, as the requestor of the read-exclusive transaction becomes the owner) - refer to [27/64 - 28/11] of Singhal as discussed above with reference to claim 1.

As per claim 5, the ownership responsibility corresponding to the coherency unit (e.g. memory line) cached by the processing subsystem transitions (i.e. loses ownership) in response to the processing subsystem receiving a corresponding address packet (which corresponds to a read-exclusive request sent by a requesting node) via the address network (specifically switch 112 that receives an invalidation request that uses the address packet to forward the invalidation to the processing subsystem - ¶171). As another node has requested ownership for the memory line, the directory associated with the home node containing this processing subsystem is updated to indicate the requesting node's ownership when the invalidation (e.g. corresponding address packet) is sent on the address network - ¶172.

As per claim 6, the address packet is part of a read-to-own transaction astaught by Singhal [27/64-66] and discussed in the rejection of claim 1 above.

As per claim 7, the read-to-own transaction (read-exclusive request) is initiated by the processing subsystem conveying the address packet on the address network - step 1200 of figure 12A and ¶170.

As per claim 8, the interface (specifically the RPE 124) is configured to forward a read-to-own message corresponding to the address packet (i.e. the read-exclusive address request) to the additional interface via the inter-node network 134 in response to receiving the address packet - ¶170. The received request is forwarded to the home node, where additional processing takes place as taught in ¶170.

As per claim 9, the coherency unit is not mapped by any memory subsystem included in the node and wherein the additional node is a home node for the coherency unit. This can be seen as the request must be forwarded to the home node for the memory line in order to obtain the data ¶¶171-172.

As per claim 10, the Examiner is considering the intra-chip switch interfaces (herein "ISI") 156 of the processing subsystems (refer to figure 3) to be part of the address network as the ISI is responsible for communication and message passing between switch 112 and the processor subsystem (106,108, and 110) - ¶61. In response to the address packet portion (e.g. the read-exclusive request's inherent address portion, as a receiving node must know what data is being requested in order to fulfill the read-exclusive request thereby making the address packet an inherent portion of a read-exclusive transaction) of a read-exclusive request being sent from the processing subsystem (¶170 and figure 12A, step 1200) and received via the output queue 162 of the address network (figure 3 and ¶61), a memory subsystem (output queue 162) included in the node is configured to send a data packet (e.g. a packet encoded as a read-exclusive request that contains the requested memory address as well as an indication that the processor 106 requests exclusive access as opposed to read/share access (¶159), as the processor 106 is responsible for initializing such a request - ¶170) indicating the read-to-own (read-exclusive) transaction to the interface (specifically, the switch 112 portion of the interface as defined supra), wherein the interface (specifically, the RPE 124) is configured to forward a read-to-own message on the inter-node network 134 (i.e. to the home node for the memory line) in response to receiving the data packet indicating the read-to-own transaction (¶170).

As per claim 11, the additional interface (in this case the home node's interface) is configured to receive the read-exclusive message via the inter-not network 134 (¶171) and to responsively send an invalidating address packet on the additional address network (as defined supra) (¶171 - where the invalidating address packet is sent to the L2 cache to invalidate the memory line in the caches of the home node). The limitation of lines 4-6 are not specifically taught by Gharachorloo as the Examiner has shown that an access right to a memory line is obtained after gaining ownership; therefore, it can be seen that a processing subsystem may never have an access right to not ownership responsibility for a memory line. Nonetheless, as this limitation is drafted in the alternative, and therefore may not necessarily occur with regards to Applicant's claimed invention, the limitation is met by Gharachorloo.

As per claim 12, wherein in response to receiving the invalidating address packet on the additional address network, the additional interface is configured to send via the inter-node network 134 a message indicating that copies of the coherency unit (memory line) in the additional node (i.e. the home node) have been invalidated to the interface (¶172). The reply sent from the home node to the requesting node, which includes the memory line, includes the number of invalidation acknowledgements that are outstanding from other nodes. This message thereby indicated that the copies of the data cached in the home node have been invalidated.

As per claim 13, the additional interface is configured to send an additional address packet on the address network (e.g. the address packet used to invalidate the cache of the processor caches 108,110), wherein if the additional processing system has an ownership responsibility associated with the coherency unit, the additional processing system is configured to transition the ownership responsibility (e.g. invalidate its copy) upon receiving the additional

address packet (¶171). Such a transition is reflected in the directory 180 which contains ownership responsibilities for all processing subsystems of a given node - see ¶66 and ¶75.

As per claim 14, wherein the additional processing system is configured to send a data packet corresponding to the coherency unit to the additional interface in response to receiving the additional address packet (e.g. the up-to-date memory line is sent from the owner node to the requesting node - ¶178), wherein the additional processing subsystem is configured to transition an access right (i.e. invalidate its cached copy of the requested data) associated with the coherency unit in response to sending the data packet corresponding to the coherency unit - ¶178.

As per claim 17, Singhal teaches the access right to the coherency unit cached by the processing subsystem (in this case the coherency unit is buffered in a bcopy buffer or a streaming I/O buffer as will be described) transitions in response to the processing subsystem receiving a data packet via the data network [28/10-11], wherein the data packet is provided to the processing subsystem as part of a write stream transaction [16/49 - 17/7] initiated by the processing subsystem. Here, the initiating processing subsystem is the "initiator" and the processing subsystem considered to be the "home node" of the requested data is the "responder."

As per claim 18, the data packet is an encoded acknowledgement (data packet sent from the responder is encoded to only contain the DataID when ready to accept the data - [16/66 - 17/4]) that excludes data (only the DataID is sent as discussed) corresponding to the coherency unit (e.g. cache line).

As per claim 20, Singhal teaches the address packet and the data packet are part of a transaction (Read-to-Own) initiated by the processing subsystem - [14/19-67], wherein the transaction also includes an additional address packet (local address packet once received over

the omnibus 30 - [14/32-34]) sent on the additional address network (the responder's (e.g. cache line owner) portion of its address bus (portion of line buses 40) and at least one message sent on the inter-node network 30 - the asserting of the Owned signal and the fulfilling of a response from the owner processor [14/40-42].

As per claim 22, Gharachorloo teaches (figure 12B, steps 1226-1230 and figure 12C, steps 1232-1234) that the additional interface (e.g. the home node's interface, specifically the HPE 122 portion of the interface) broadcasts an invalidation address packet on the additional address network (this can be seen since if one of its processors 106 contains the cache line, the address must be sent to that processor via the data bus portion of switch 122 in order to invalidate the cache line). Singhal also teaches broadcasting the address on the address bus in order to invalidate the cache line in the other sharing processors - [28/31-34].

As per claim 23, Gharachorloo teaches the sending back of the invalidation acknowledgments from the additional interface to the interface (of the requesting node), wherein the message indicates that the shared copies have been invalidated at the additional node (¶¶180-181). Singhal teaches that if the additional processing subsystem has an access right (e.g. is an author) to but not an owner of the cache line (could not be during a readtoown as ownership is transferred at the time of request - [27/64-66]), the additional processing subsystem is configured to transition the access right to the coherency unit (cache line) upon receipt of the invalidating address packet [28/3-11].

As per claim 24, Singhal teaches the transaction is a read-to-own transaction [14/17-67], wherein the processing subsystem is configured to initiate the read-to-own transaction by sending a read-to-own packet on the address network [12/47 - 13/5].

As per claim 25, Singhal teaches wherein no memory subsystem (i.e. memory 150) included in the node (i.e. the requesting node) maps the coherency unit (i.e. the memory line is mapped to another node or device 50) - [14/28-39] and [22/1-19], wherein in response to the read-to-own packet on the address network, the interface (elements 140 and 180) is configured to send a read-to-own message to the additional interface in the additional node (messages sent via the omnibus 30 in a broadcast method - [12/47-62].

As per claim 26, Gharachorloo teaches the address network (specifically the switch 112) is configured to convey the address packet (e.g. the address portion of the read-exclusive request packet) from a directory (e.g. a Dtag array) to the processing subsystem (i.e. when the address is used to invalidate data cached locally that is associated with a received read-exclusive request) in a point-to-point mode (this can be seen since the invalidation is only sent to those processing subsystems (e.g. combination 106,108, and 110) which contain the data corresponding to the read-exclusive request via switch 112) - ¶171. The Dtag array is used to locate which processor caches contain the data to be invalidated from the received address packet, and the L2 cache executes a point-to-point invalidation request using the address packet (i.e. the address packet inherently must be sent as it contains the address of the associated memory line to be invalidated) to only those caches 108,110 that contain the associated data.

As per claim 27, Singhal teaches the address network conveys the address packet in broadcast mode [7/37-40].

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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